Organisasi Sistem Komputer

OSK 13 – Microprogrammed Control

Muh. Izzuddin Mahali, M.Cs.

Micro-programmed Control

- Use sequences of instructions (see earlier notes) to control complex operations
- Called micro-programming or firmware

Implementation (1)

- All the control unit does is generate a set of control signals
- Each control signal is on or off
- Represent each control signal by a bit
- Have a control word for each micro-operation
- Have a sequence of control words for each machine code instruction
- Add an address to specify the next micro-instruction, depending on conditions

Implementation (2)

- Today's large microprocessor
  - Many instructions and associated register-level hardware
  - Many control points to be manipulated
- This results in control memory that
  - Contains a large number of words
    - co-responding to the number of instructions to be executed
  - Has a wide word width
    - Due to the large number of control points to be manipulated

Micro-program Word Length

- Based on 3 factors
  - Maximum number of simultaneous micro-operations supported
  - The way control information is represented or encoded
  - The way in which the next micro-instruction address is specified

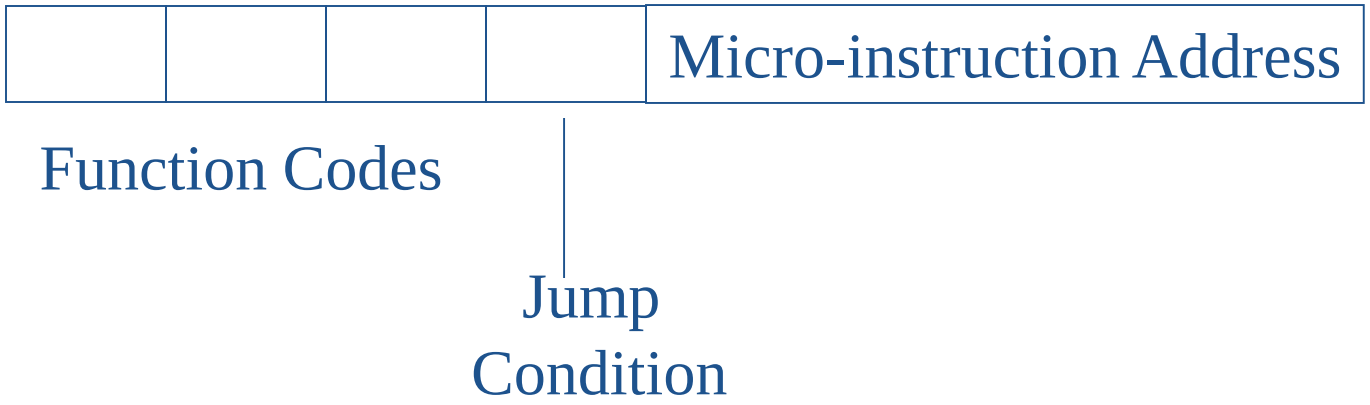
Micro-instruction Types

- Each micro-instruction specifies single (or few) micro-operations to be performed
  - (*vertical* micro-programming)
- Each micro-instruction specifies many different micro-operations to be performed in parallel
  - (*horizontal* micro-programming)

Vertical Micro-programming

- Width is narrow
- n control signals encoded into $\log_2 n$ bits
- Limited ability to express parallelism
- Considerable encoding of control information requires external memory word decoder to identify the exact control line being manipulated

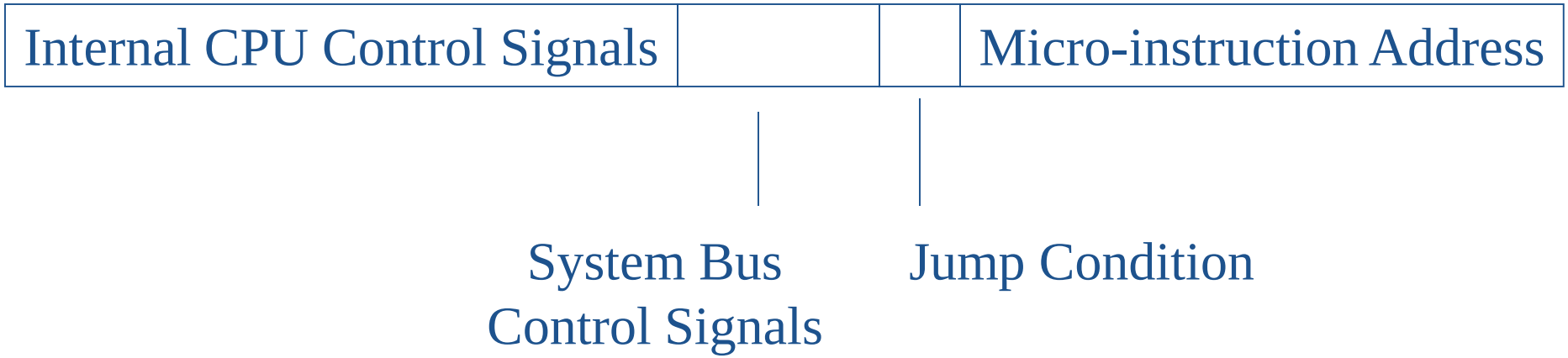
Vertical Micro-programming diag



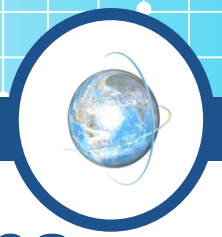
Horizontal Micro-programming

- Wide memory word
- High degree of parallel operations possible
- Little encoding of control information

Horizontal Micro-programmed diag

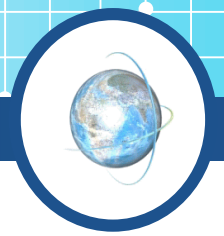


Compromise



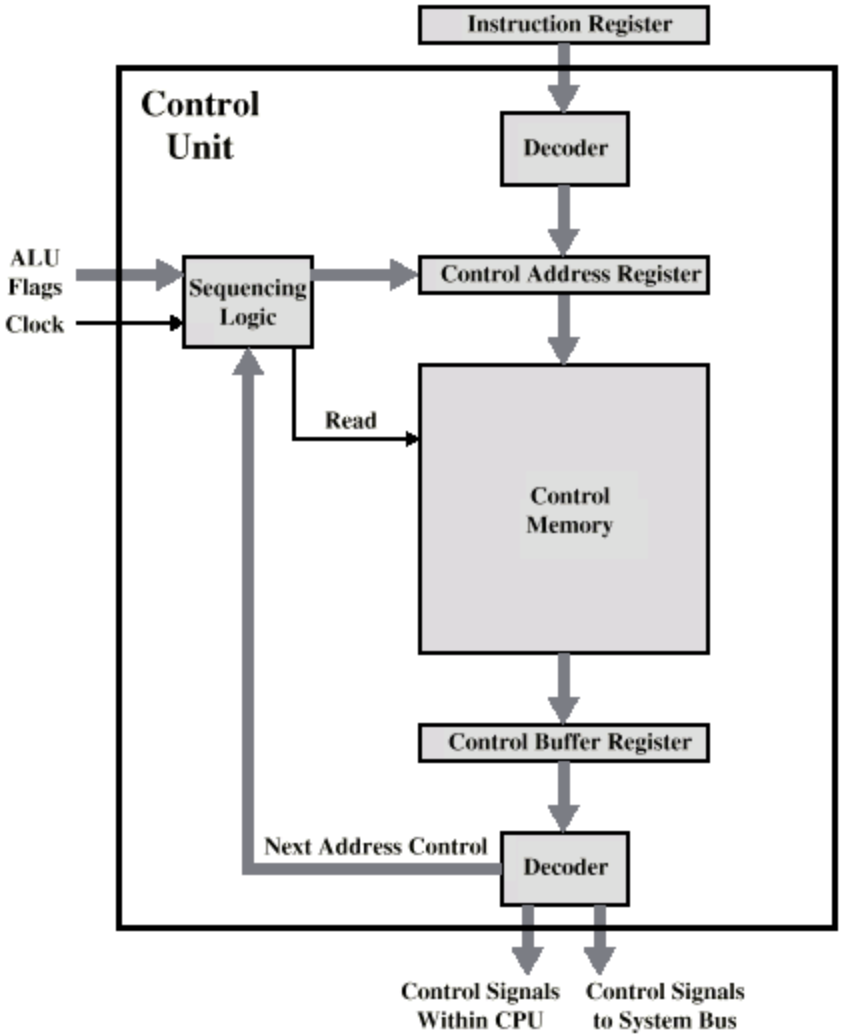
- Divide control signals into disjoint groups
- Implement each group as separate field in memory word
- Supports reasonable levels of parallelism without too much complexity

Control Memory

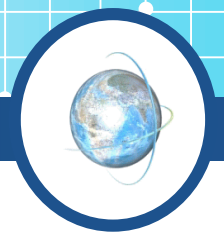


. Jump to Indirect or Execute	Fetch cycle routine
. Jump to Execute	Indirect Cycle routine
. Jump to Fetch	Interrupt cycle routine
Jump to Op code routine	Execute cycle begin
. Jump to Fetch or Interrupt	AND routine
. Jump to Fetch or Interrupt	ADD routine

Control Unit



Control Unit Function



- Sequence login unit issues read command
- Word specified in control address register is read into control buffer register
- Control buffer register contents generates control signals and next address information
- Sequence login loads new address into control buffer register based on next address information from control buffer register and ALU flags

Advantages and Disadvantages

- Simplifies design of control unit
  - Cheaper
  - Less error-prone
- Slower

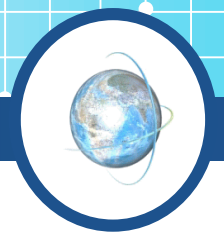
Tasks Done By Microprogrammed Control Unit

- Microinstruction sequencing
- Microinstruction execution
- Must consider both together

Design Considerations

- Size of microinstructions
- Address generation time
  - Determined by instruction register
    - Once per cycle, after instruction is fetched
  - Next sequential address
    - Common in most designed
  - Branches
    - Both conditional and unconditional

Sequencing Techniques



- Based on current microinstruction, condition flags, contents of IR, control memory address must be generated
- Based on format of address information
  - Two address fields
  - Single address field
  - Variable format

Address Generation

- Explicit
- Two-field
- Unconditional Branch
- Conditional branch

Implicit

Mapping

Addition

Residual control

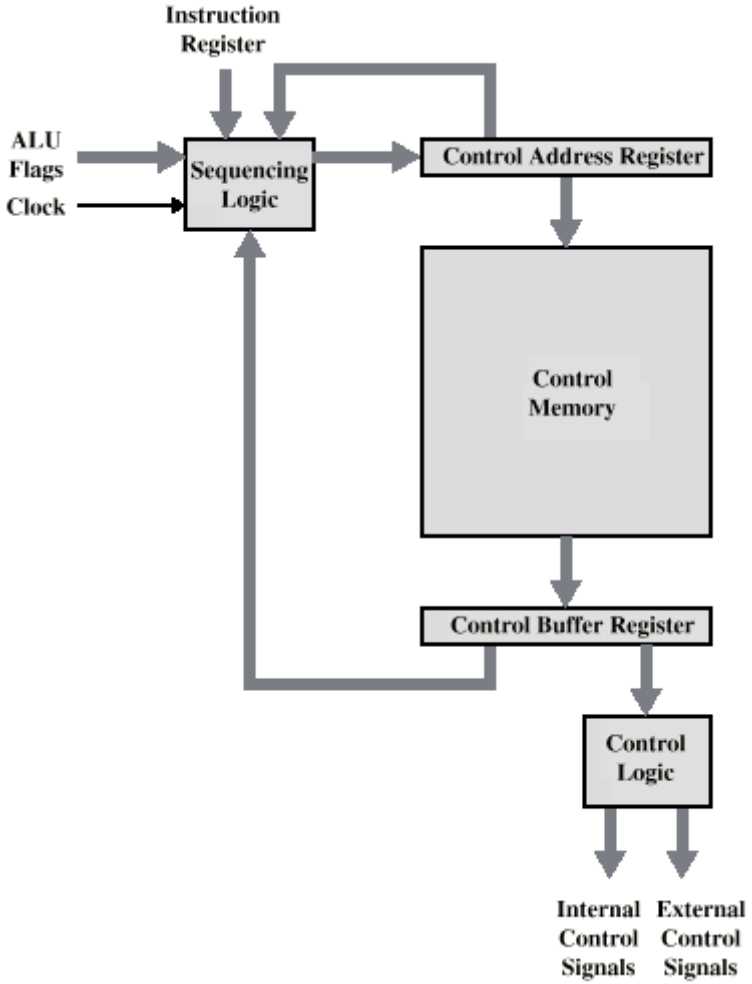
Execution

- The cycle is the basic event
- Each cycle is made up of two events
  - Fetch
    - Determined by generation of microinstruction address
  - Execute

Execute

- Effect is to generate control signals
- Some control points internal to processor
- Rest go to external control bus or other interface

Control Unit Organization



Required Reading

- Stallings chapter 15